What is claimed:

1. In a gate structure of a semiconductor device constructed by a gate oxide layer, a polysilicon layer, a tungsten layer, a tungsten nitride layer, a nitride layer and an anti-reflection layer, the gate structure of the high integration semiconductor device comprising:

an etching prevention layer formed between the anti-reflection layer and the nitride layer that prevents the etching of the tungsten layer and the tungsten nitride layer.

2. The gate structure according to claim 1, wherein the etching prevention layer is titanium or titanium nitride.

3. A method for forming a gate electrode of high integration semiconductor device comprising the steps of:

sequentially depositing a gate oxide layer, a polysilicon layer, a tungsten nitride layer, a tungsten layer, and a nitride layer on the semiconductor substrate to form a resultant material on the semiconductor substrate;

depositing an etching prevention layer and an anti-reflection layer sequentially on the resultant material;

forming a pattern by depositing a photoresist layer on the anti-reflection layer and executing a mask process;

etching the nitride layer, the tungsten layer and the tungsten nitride layer sequentially with an etching gas comprising fluorine; and

etching the etching prevention layer and the polysilicon layer with an etching gas comprising chlorine.

4. The method for forming a gate according to claim 3, wherein the etching prevention layer has a thickness ranging from about 50 to about 1000Å.

5. The method for forming a gate according to claim 3, wherein the etching gas comprising fluorine is selected from the group consisting of NF_3, SF_6 and CF_4 gases.

6. A semiconductor device comprising:

a semiconductor substrate,

a gate structure disposed on the semiconductor substrate, the gate structure comprising a gate oxide layer disposed on the semiconductor substrate,

a polysilicon layer disposed on the gate oxide layer, a tungsten layer disposed on the polysilicon layer,

a tungsten nitride layer disposed on the tungsten layer,

a nitride layer disposed on the tungsten nitride layer,

an etching prevention layer disposed on the nitride layer, and

an anti-reflection layer disposed on the etching prevention layer.

7. The semiconductor device of claim 6, wherein the etching prevention layer is titanium or titanium nitride.

8. A method for forming a gate electrode of a high integration semiconductor device comprising the steps of:

providing a semiconductor substrate,

sequentially depositing a gate oxide layer,a polysilicon layer, a tungsten nitride layer, a tungsten layer and a nitride layer on the semiconductor substrate,

depositing an etching prevention layer on the nitride layer,

forming a pattern by depositing a photoresist layer on the anti-reflection layer using a mask process,

etching the nitride layer, the tungsten layer and the tungsten nitride layer sequentially with an etching gas comprising fluorine, and

etching the etching prevention layer and the polysilicon layer with an etching gas comprising chlorine.

9. The method of claim 8, wherein the etching prevention layer has a thickness ranging from about 50 to about 1000 Å.

10. The method of claim 8, wherein the etching gas comprising fluorine is selected from the group consisting of NF_3, SF_6 and CF_4 gases.